MEMORY HUB ARCHITECTURE HAVING PROGRAMMABLE LANE WIDTHS

ABSTRACT OF THE DISCLOSURE

[022] A processor-based system includes a processor coupled to a system controller through a processor bus. The system controller is used to couple at least one input device, at least one output device, and at least one data storage device to the processor. Also coupled to the processor bus is a memory hub controller coupled to a memory hub of at least one memory module having a plurality of memory devices coupled to the memory hub. The memory hub is coupled to the memory hub controller through a downstream bus and an upstream bus. The downstream bus has a width of M bits, and the upstream bus has a width of N bits. Although the sum of M and N is fixed, the individual values of M and N can be adjusted during the operation of the processor-based system to adjust the bandwidths of the downstream bus and the upstream bus.